



CC2420 Errata Note 001, rev. 1.0

Active and passive scans as defined in IEEE 802.15.4 are affected by a bug in the CC2420 hardware address recognition causing beacon frames to be rejected. The bug can be avoided in software and is also fixed in the latest hardware revision.

Description and reason for the problem

Early revisions of the CC2420 hardware address recognition contains a bug, which causes beacon frames to be rejected even if the PAN ID programmed into CC2420 RAM is equal to 0xFFFF. This affects active and passive scans as defined by IEEE 802.15.4.

Suggested workaround

When performing active and passive scans on batches affected by this bug, the CC2420 hardware address recognition must be disabled in order to pass the incoming beacon frames. During active scan, a beacon request frame is transmitted before listening for beacons. During passive scan, CC2420 only listens for beacons without performing any active transmission. For both types of scan, all incoming non-beacon frames shall be rejected (section 7.5.2.1 in IEEE 802.15.4). This rejection must be implemented in MAC software.

When performing active and passive scans on production samples of CC2420 (batches not listed below), make sure that the IOCFG0.BCN_ACCEPT control bit is set while doing active and passive scan. This control bit is not available in chips from the batches listed in the "Batches affected" section below.

Fix

Implementing a software workaround in the MAC SW solves this problem.

Batches affected

This errata note applies to prototype chip batches marked W61135.00 and W61135.01. These batches also have the MANFIDH.VERSION register bits set to 0 and 1 respectively. Batches not affected have the MANFIDH.VERSION register bits set to 2 or higher.

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Document History

Revision	Date	Description/Changes
1.0	2004-03-19	First edition.







CC2420 Errata Note 002, rev. 2.0

March 18, 2005

For CC2420 devices marked with lot codes ranging from WA8402.00 to WB8341.00 correct operation of the SPI interface is not guaranteed at I/Ovoltages below 2.1 V, unless the on-chip voltage regulator is used. This problem is now fixed and operation down to 1.6 V is ensured for devices with lot codes succeeding WB8341.00.

Description and reason for the problem

When using I/O-voltages below 2.1 V a limitation in the digital pads has been observed to cause reduced SPI speed and in some cases loss of functionality. This will only occur for I/O pins configured as inputs and at I/O-voltages below 2.1 V.

Suggested workaround

Using I/O-voltages at or above 2.1 V will ensure reliable operation and unaffected SPI speed. Designs already utilizing the CC2420 on-chip voltage regulator will comply with this requirement.

Fix

Using the CC2420 on-chip regulator or voltages above 2.1 V solves the problem for those devices affected.

Batches affected

This errata note applies to all CC2420 devices marked with lot codes ranging from WA8402.00 through WB8341.00. For devices with lot codes succeeding WB8341.00 this problem is resolved.

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Document History

Revision	Date	Description/Changes
2.0	2005-03-18	Problem fixed on lot codes higher than WB8341.00
1.0	2004-10-18	Initial release





CC2420 Errata Note 003, rev. 0.3

March 18, 2005

For CC2420 devices marked with lot codes ranging from WA8402.00 to WB8341.00 operation using VDD supply voltages below 1.8 V can lead to packet loss. This problem, which occurs mainly at low temperatures, is now fixed and operation down to 1.6 V is ensured for devices with lot codes succeeding WB8341.00.

Description and reason for the problem

When supplying the 1.8 V VDD supply pins (pins no. 1, 2, 3, 4, 10, 14, 15, 17, 18, 20, 26, 35, 37, 44, 48) with voltages below 1.8 V, oscillations in the receive filter has been observed for some devices. This phenomenon has mainly been observed at low operating temperatures, and will lead to degraded or non-functional signal reception. Applications using the internal regulator at room temperature or above are unlikely to encounter this issue.

Suggested workaround

This issue is corrected in CC2420 with lot codes succeeding WB8341.00. In order for the fix to work properly, the following register setting must be used during receive mode:

[RXCTRL1.RXBPF LOCUR] = 1

This setting will reduce the RX current consumption by approximately 1.2 mA, and is compatible with previous versions of the CC2420.

Chipcon's IEEE 802.15.4 MAC will support this setting from version 0.71.

No workaround exists for CC2420 versions with lot codes between WA8402.00 and WB8341.00.

Fix

Using CC2420 with lot codes succeeding WB8341.00, in conjunction with the suggested register setting, fixes the issue.

Batches affected

CC2420 devices marked with lot codes WA8402.00 through WB8341.00 are affected by this problem. For devices with lot codes succeeding WB8341.00 this problem is resolved.

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Document History

Revision	Date	Description/Changes
1.0	2005-03-18	Initial release