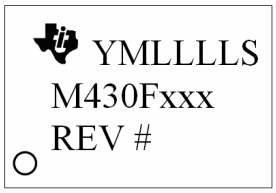
MSP430F15x/16x/161x Device Errata Sheet
Current Version

Devices	Rev:	CPU4	I2C7	TA12	TB2	US15	WDG2
MSP430F155	D	✓	✓	✓	✓	✓	✓
MSP430F156	D	✓	✓	✓	✓	✓	✓
MSP430F157	D	✓	✓	✓	✓	✓	✓
MSP430F167	D	✓	✓	✓	✓	✓	✓
MSP430F168	D	✓	✓	✓	✓	✓	✓
MSP430F169	D	✓	✓	✓	✓	✓	✓
MSP430F1610	B	✓	✓	✓	✓	✓	✓
MSP430F1611	B	✓	✓	✓	✓	✓	✓
MSP430F1612	B	✓	✓	✓	✓	✓	✓

Note: See Appendix for prior revisions

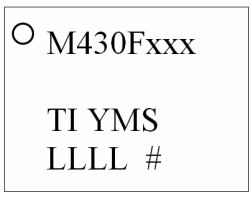
Package Markings

PM64: LQFP(PM) 64-pin



YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision
o = PIN 1

RTD64: QFN(RTD) 64-pin



TI = TI
YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision
o = PIN 1

Detailed Bug Description

CPU4 CPU4 - Bug description:

Module: CPU, Function PUSH #4, PUSH #8

The single operand instruction PUSH cannot use the internal constants (CG) 4 and 8. The other internal constants (0, 1, 2, -1) can be used. The Assembler version 1.08 and higher produces correct code. The number of clock cycles is different:
PUSH #CG uses address mode 00, requiring 3 cycles, 1 word instruction
PUSH #4/#8 uses address mode 11, requiring 5 cycles, 2 word instruction

Workaround implemented in assembler.
No fix planned.

I2C7 I2C7 - Bug description:

Module: USART (I2C Mode): ARDYIFG Interrupt flag is not generated.

When the USART is configured for I2C communication (U0CTL[5]=1, U0CTL[2]=1, U0CTL[0]=1) and the I2C is configured as a system slave (U0CTL[1]=0), the ARDYIFG interrupt flag generation can fail to generate, even when both the Stop condition is received and the receive buffer is empty.
This condition occurs when the I2C clock source, selected by I2CTCTL[5-4], is disabled by the Status Register (SR) control signals OSCOFF or SCG1.
In this configuration, the hardware clock activation is enabled by the I2C module. However, if RXRDYIFG is polled for data buffer reception, the I2C hardware clock activation may be disabled before the ARDYIFG is generated.

Workaround:
Solution #1: Use interrupt service routines via the I2C_IV to handle all I2C interrupts.
Solution #2: After detection of I2C Own Address (OAIFG), the selected I2C clock source is enabled by clearing the OSCOFF or SCG1 Status Register (SR) bits. When the ARDYIFG is detected, the OSCOFF or SCG1 in the Status Register (SR) can be set to disable the clock source and return to the desired low power mode operation.
Solution #3: For slave only devices, it is normally not necessary to use ARDYIFG.

TA12 TA12 - Bug description (same as TB2):

Module: TimerA, Interrupt is lost (slow ACLK)

TimerA counter is running with slow clock (external TACLK or ACLK) compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by 1 with the occurring compare interrupt (if TAR = CCRx).
Due to the fast MCLK the CCRx register increment (CCRx = CCRx+1) happens before the TimerA counter has incremented again. Therefore the next compare interrupt should happen at once with the next TimerA counter increment (if TAR = CCRx + 1). This interrupt gets lost.

Workaround:
Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterwards.

Detailed Bug Description (continued)

TB2 TB2 - Bug description (same as TA12):

Module: TimerB, Interrupt is lost (slow ACLK)

TimerB counter is running with slow clock (external TBCLK or ACLK) compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by 1 with the occurring compare interrupt (if TBR = CCRx).
Due to the fast MCLK the CCRx register increment (CCRx = CCRx+1) happens before the TimerB counter has incremented again. Therefore the next compare interrupt should happen at once with the next TimerB counter increment (if TBR = CCRx + 1). This interrupt gets lost.

Workaround:
Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterwards.

US15 US15 - Bug description:

Module: USART0, USART1, Function: UART receive with two stop bits

USART hardware does not detect a missing second stop bit when SPB = 1. The Framing Error Flag (FE) will not be set under this condition and erroneous data **reception may occur**.

Workaround:
None (Configure USART for a single stop bit, SPB = 0)

WDG2 WDG2 - Bug description:

If a key violation is caused by erroneously accessing a flash control register, the watchdog interrupt flag is set in addition to a correctly generated PUC.

Workaround:
None

Appendix: Prior Versions

Devices	Rev:	CPU4	I2C7	SVS2	TA12	TB2	US14	US15	WDG2	XOSC4
MSP430F155	D	✓	✓		✓	✓		✓	✓	
	C	✓	✓	✓	✓	✓	✓	✓	✓	
	B	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F156	D	✓	✓		✓	✓		✓	✓	
	C	✓	✓	✓	✓	✓	✓	✓	✓	
	B	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F157	D	✓	✓		✓	✓		✓	✓	
	C	✓	✓	✓	✓	✓	✓	✓	✓	
	B	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F167	D	✓	✓		✓	✓		✓	✓	
	C	✓	✓	✓	✓	✓	✓	✓	✓	
	B	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F168	D	✓	✓		✓	✓		✓	✓	
	C	✓	✓	✓	✓	✓	✓	✓	✓	
	B	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F169	D	✓	✓		✓	✓		✓	✓	
	C	✓	✓	✓	✓	✓	✓	✓	✓	
	B	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F1610	B	✓	✓		✓	✓		✓	✓	
	A	✓	✓	✓	✓	✓	✓	✓	✓	
MSP430F1611	B	✓	✓		✓	✓		✓	✓	
	A	✓	✓	✓	✓	✓	✓	✓	✓	
MSP430F1612	B	✓	✓		✓	✓		✓	✓	
	A	✓	✓	✓	✓	✓	✓	✓	✓	

Detailed Bug Description

SVS2 SVS2 - Bug description:

Module: SVS, DAC1: DAC1 overrides the input of the SVS comparator

DAC1 overrides the input of the SVS comparator. This is caused by a conflict between SVS and DAC1 at Port 6.7. DAC1 is enabled when DAC12AMPx is > 0.

Workaround:
Do not enable DAC1 when the SVS is used.

US14 US14 - Bug description:

Module: USART0, USART1, UART Mode: Lost character start edge

When using the USART in UART mode with UxBR0 = 0x03 & UxBR1 = 0x00, the start edge of received characters may be ignored due to internal timing conflicts within the UART state machine. This condition does not apply when UxBR0 is > 0x03.

Workaround:
None

XOSC4 XOSC4 - Bug description:

Module: XT1: XT1 high frequency oscillator low power wake-up error

The XT1 high frequency oscillator wake-up from low power mode operation is not functional.

Workaround:
If using the XT1 high frequency oscillator circuitry (XTS, BCSCTL1[6] = 1), the OSCOFF bit in the Status Register (SR) must always = 0.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265